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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,994	02/25/2004	Richard P. Schubert	A0312.70523US00	4477

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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,994	SCHUBERT ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 30-36* is/are pending in the application.

4a) Of the above claim(s) *14-29* is/are withdrawn from consideration.

5)☒ Claim(s) *1-13* is/are allowed.

6)☒ Claim(s) *30 and 34-36* is/are rejected.

7)☒ Claim(s) *31-33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/21/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Applicant's election without traverse of claims 14-29 is cancelled, and claims 1-13 and 30-36 are pending in the application in the reply filed on 06/30/2006 is acknowledged. Thus, this Office action is in response to claims 1-13 and 30-36.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 07/21/2004 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Syed et al., US 2002/0108021 A1.

Regarding claim 34, Syed teaches a digital signal processor comprising:

a core processor (core processor 102 as shown in Fig.1);

a level one memory (it is taught as cache memory 104) for operation with the core processor;

a first buffer (it is taught as a store buffer 210 in Fig.2) configured to hold write information, received from the core processor, for the level one memory (section 0033, lines 1-12);

a second buffer (it is taught as a write buffer 216) configured to hold write information, received from the core processor, for a level two memory (section 0036, level two memory is considered as main memory); and

a memory controller (it is taught as a cache memory controller 208) configured to steer the write information to the first buffer or the second buffer based on an address of a write operation (section 0033, lines 1-10 and section 0036, lines 11-17).

Regarding claim 35, Syed teaches the first and second buffers each comprise a Store buffer and a write buffer (it is taught as receiving the write information from one of the register of the processor and is stored in the store buffer, and receiving the write information from one of the register of the processor and is store in the store buffer and further is stored to the write buffer, section 0022, 0033 and 0036).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 30 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Syed et al., US 2002/0108021 A1, and in view of Nanda et al., US 6,038,645

Regarding claim 30, a digital signal processor comprising:

a core processor a core processor (core processor 102 as shown in Fig.1);

a first write buffer (it is taught as a stored buffer 210) configured to hold write information, received from the store buffer (it is taught as write information is received from the processor which includes a register, Fig.1 and section 0022), for a level two memory (a level two memory is considered as cache 104, see section 0033);

a second write buffer (it is taught as a write buffer 216) configured to hold write information, received from the store buffer (it is taught as write information is received from the processor which includes a register, Fig.1 and section 0022, and write information is stored in the store buffer and to the write buffer), for a level three memory(a level memory is considered as a main memory, section 0036); and

a memory controller (it is taught as a cache memory controller 208) configured to steer the write information to the first buffer or the second buffer based on an address of a write operation (section 0033, lines 1-10 and section 0036, lines 11-17).

Syed does not clearly teach that a level one memory for operation with the core processor and a store buffer configured to hold write information, generated by the core processor; he only mentioned that there are registers in the core processor 102 (section 0022).

However, Nanda teaches that a microprocessor 10 includes a CPU core, a combined storage queue 16, cache memory 18 and memory 18, all storage memories are connected by a bus 14 as shown in Fig.1, Nanda also teaches CPU core 12 outputs information which is intended to be written to at least one level of the microprocessor storage system (col.2, last three lines).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Nanda into Syed's system such as a microprocessor includes a cache memory for operation with the core processor and a store buffer configured to hold write information because one or more hierarchical levels of storage within a microprocessor will provide greater overall microprocessor speed while maximizing efficient (col.1, lines 16-40 of Nanda).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 36, Syed does not teach further comprising a third buffer configured to hold write information, received from the core processor, for a level three memory.

However, Nanda teaches that a microprocessor 10 includes a CPU core, a combined storage queue 16, cache memory 18, the cache memory can be multiple cache levels (see col.3, lines 25-27 of Nanda) and memory 18. all storage memories are connected by a bus 14 as shown in Fig.1, Nanda also teaches CPU core 12 outputs information which is intended to be written to at least one level of the microprocessor storage system (col.2, last three lines).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Nanda into Syed's system such as various hierarchical levels of storages which includes the third buffer hold write information for the level three memory because one or more hierarchical levels of storage within a microprocessor will provide greater overall microprocessor speed while maximizing efficient (col.1, lines 16-40 of Nanda).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Allowable Subject Matter

9. Claims 1-13 allowed.

10. Claims 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest that a memory controller configured to enable the excess capacity of the write buffer wherein the write buffer having a normal capacity and an excess capacity when a high priority task is being serviced and to inhibit write access to the excess capacity of the write buffer when a high priority task is not being serviced as claimed in claim 1,8,13 and 31 in combination with the other elements set forth in the claimed invention.

Claims 32-33 are allowable as being dependent upon claim 31 and having additional allowable features therein.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Birk et al	US 2003/0061445 A1
Gaskins et al	US 6553473 B1
Jamil et al	US 2003/0126365 A1
Rhoden et al	US 6008823
Moyer et al	US 6976110 B2

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Patent Examiner

August 21, 2006